PXIe-5624 Specifications

2025-09-22

Contents

NI PXIe-5624R Specifications

PXIe-5624 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are ***Warranted*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Internal Reference Clock source is used.
- Dither level is set to high.
- Digital downconversion (DDC) mode enabled.

Warranted specifications are valid under the following conditions unless otherwise noted.

- 20 minutes warm-up time after the chassis is powered on and the LabVIEW Instrument Design Libraries for IF Digitizers software is loaded and recognizes the PXIe-5624. The warm-up time ensures that the PXIe-5624 and test instrumentation are at a stable operating temperature.
- Calibration cycle is maintained.
- Calibration IP is used properly during the creation of custom FPGA bitfiles.[1]

- Chassis fan speed is set to high. In addition, NI recommends using slot blockers and EMC filler panels in empty module slots to minimize temperature drift.

PXIe-5624 Pinout

Use the pinout to connect to terminals on the PXIe-5624.

Figure 1. PXIe-5624 Connector Pinout

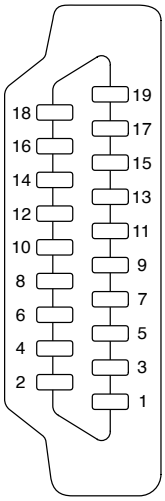


Table 1. PXIe-5624 Signal Descriptions

Pin	Signal Name	Description
1	DIO (0)	Bidirectional single-ended (SE) digital I/O (DIO) data channel.
2	GND	Ground reference for signals.
3	DIO (1)	Bidirectional SE DIO data channel.
4	DIO (2)	Bidirectional SE DIO data channel.
5	GND	Ground reference for signals.
6	DIO (3)	Bidirectional SE DIO data channel.
7	DIO (4)	Bidirectional SE DIO data channel.
8	GND	Ground reference for signals.
9	DIO (5)	Bidirectional SE DIO data channel.
10	DIO (6)	Bidirectional SE DIO data channel.
11	GND	Ground reference for signals.

1. Refer to the ***NI IF Digitizers Help*** for more information about calibration IP.

Pin	Signal Name	Description
12	DIO (7)	Bidirectional SE DIO data channel.
13	DIO (8)	Bidirectional SE DIO data channel.
14	NC	No connect.
15	DIO (9)	Bidirectional SE DIO data channel.
16	DIO (10)	Bidirectional SE DIO data channel.
17	GND	Ground reference for signals.
18	+5 V	+5 V power (10 mA maximum).
19	DIO (11)	Bidirectional SE DIO data channel.

Modes of Operation

The PXIe-5624 is a software designed instrument with a user-programmable FPGA.

The LabVIEW Instrument Design Libraries for IF Digitizers includes example FPGA images to use the PXIe-5624 in two modes of operation.

- **Digitizer Mode**—Data from the ADC is stored directly into DRAM on the PXIe-5624 and fetched from the host. This data is not equalized or calibrated.
- **Digital Downconversion (DDC) Mode**—Data from the ADC goes through signal processing before being stored in DRAM. The data is shifted in frequency, decimated, equalized, and calibrated using digital signal processing (DSP) on the FPGA.

Frequency

Input frequency range (3 dB bandwidth)	5 MHz to 2 GHz, typical[2]
Equalized bandwidth	
400 MHz acquisition FPGA image[3][3]	95 Hz to 400 MHz

2. Refer to Frequency Response for more information about this specification.
3. Refer to the NI PXIe-5624R Getting Started Guide for more information about FPGA images.

800 MHz acquisition FPGA image[3]	800 MHz

Note The equalized bandwidth cannot cross Nyquist boundaries:
5 MHz ≤ ***DDC Center Frequency*** ± BW/2 ≤ 1 GHz,
1 GHz ≤ ***DDC Center Frequency*** ± BW/2 ≤ 2 GHz

Bandwidth resolution (400 MHz acquisition FPGA image[3])	3.56 µHz
Frequency shift resolution	7.13 µHz
Dither frequency range	1 MHz to 50 MHz, typical

Internal Frequency Reference

Initial adjustment accuracy	$\pm 0.2 \times 10^{-6}$
Temperature stability	
23 ± 5 °C	$\pm 0.5 \times 10^{-6}$, nominal
0 °C to 55 °C	$\pm 2.0 \times 10^{-6}$, maximum
Aging	$\pm 0.5 \times 10^{-6}$ per year, maximum
Accuracy	***Initial adjustment accuracy*** ± ***Aging*** ± ***Temperature stability***

Frequency Reference/ADC Sample Clock Input (CLK IN)

Refer to CLK IN for more information about frequency reference/ADC Sample Clock input (CLK IN).

Frequency Reference/ADC Sample Clock Output (CLK OUT)

Refer to CLK OUT for more information about frequency reference/ADC Sample Clock output (CLK OUT).

Spectral Purity

Sampling jitter, nominal	
CLK OUT	172 fs RMS[4]
IF IN	172 fs RMS[5]

Table 2. Single Sideband Phase Noise[6]

Carrier Frequency (MHz)	Offset	SSB Phase Noise (dBc/Hz), Typical
187.5	100 Hz	-95
	1 kHz	-115
	10 kHz	-133
	100 kHz	-147
	1 MHz	-149
800	100 Hz	-82
	1 kHz	-103

4. Conditions: 2 GHz ADC Sample Clock integrated from 100 Hz to 10 MHz. Refer to the Measured Sampling Clock Phase Noise with an Internal Reference Clock, 2 GHz figure.
5. Conditions: 800 MHz input, locked to internal Reference Clock, integrated from 100 Hz to 10 MHz. Refer to the Measured SSB Phase Noise of Internal Reference, Multiple Frequencies figure.
6. Conditions: Dither disabled, single-tone input level of 7 dBm.

Carrier Frequency (MHz)	Offset	SSB Phase Noise (dBc/Hz), Typical
	10 kHz	-119
	100 kHz	-142
	1 MHz	-146

Figure 2. Measured SSB Phase Noise[7] at 187 MHz, Multiple Clock Configurations[8]

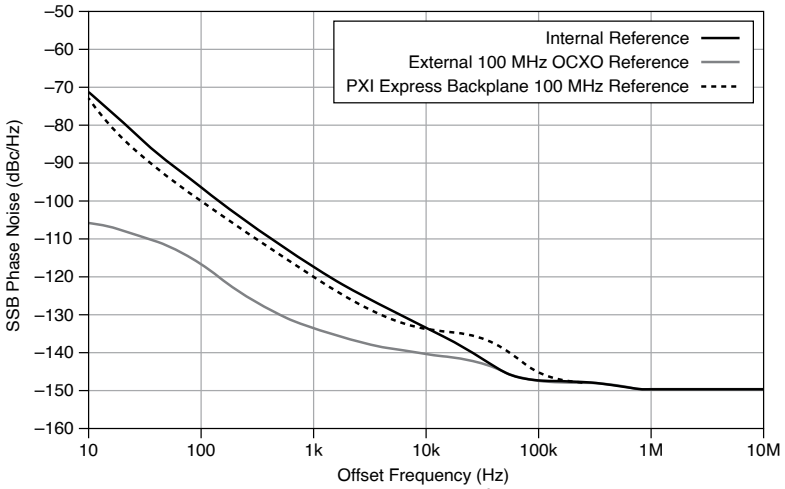
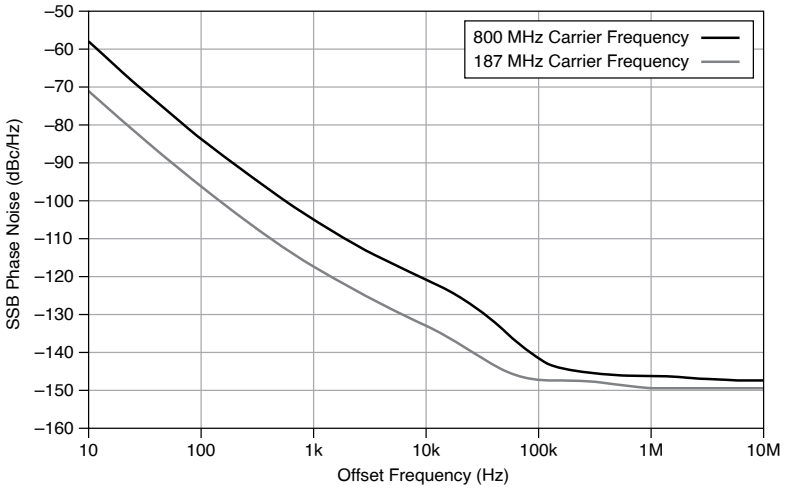
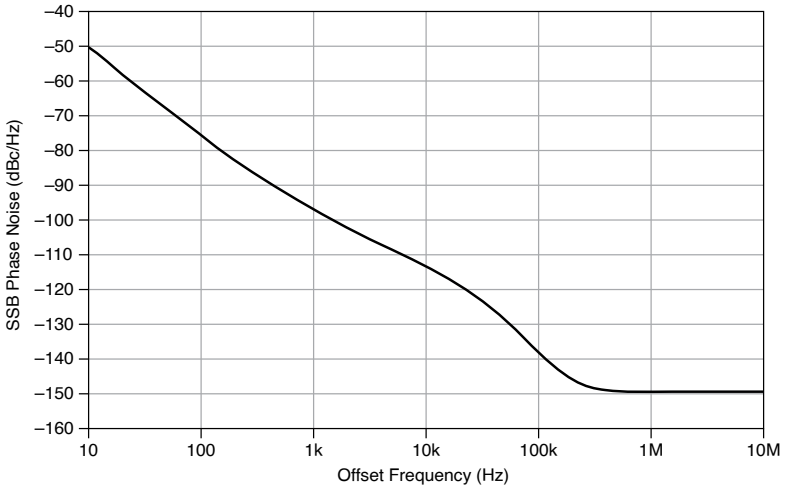


Figure 3. Measured SSB Phase Noise[9] of Internal Reference, Multiple Carrier Frequencies[10]



7. Conditions: Dither disabled, single tone input level of 7 dBm. CW spurs removed from plots. OCXO source is PXIe-5653. Backplane PXI Express 100 MHz source is an PXIe-1085 chassis.
8. Phase noise measurement at 187 MHz limited from 100 kHz to 1 MHz by signal generator.
9. Conditions: Dither disabled, single-tone input level of 7 dBm.
10. Phase noise measurement at 187 MHz limited from 100 kHz to 1 MHz by signal generator.

Figure 4. Measured Sampling Clock Phase Noise[11] with an Internal Reference Clock, 2 GHz



IF Input (IF IN)

Number of channels	1 (IF IN)

Table 3. Full-Scale Input Range

Dither Setting	Value	Value (dBm), Typical
Off	8 dBm (1.58 Vpk-pk)	9
On	6 dBm (1.26 Vpk-pk)	7

Absolute Amplitude Accuracy

Table 4. Absolute Amplitude Accuracy (dBm)[12]

Frequency	15 °C to 35 °C (Self-Calibration ± 5 °C)	0 °C to 55 °C (Self-Calibration ± 5 °C)
25 MHz to 1 GHz, dither enabled[12]	±0.25	±0.30
	±0.10, typical	±0.15, typical
1 GHz to 1.975 GHz, dither	±0.30	±0.35

11. Conditions: Measured on unit configured to export ADC Sample Clock from REF OUT when using an internal Reference Clock. CW spurs removed.
12. Conditions: Equalization filter enabled. Input power at -16 dBFS. Specification valid across entire bandwidth for bandwidths less than or equal to 400 MHz.

Frequency	15 °C to 35 °C (Self-Calibration ± 5 °C)	0 °C to 55 °C (Self-Calibration ± 5 °C)
enabled	±0.15, typical	±0.20, typical
25 MHz to 1 GHz, dither disabled	±0.20, typical	±0.25, typical
1 GHz to 1.975 GHz, dither disabled	±0.25, typical	±0.30, typical

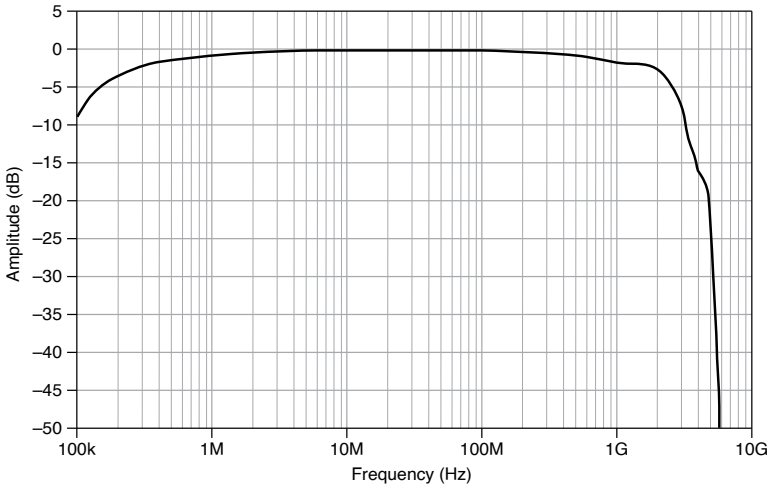
Note The absolute amplitude accuracy specification is valid only when the module is operating within the specified ambient temperature range and within the specified range from the last self-calibration temperature, as measured with the onboard device temperature sensor.

Table 5. Linearity

Input Power (dBFS)	Linearity (dB)	
	Dither ON	Dither OFF
≥-20	±0.10	—
	±0.03, measured	±0.04, measured
<-20 to >-50	±3.00	—
	±0.04, measured	±0.15, measured

Frequency Response

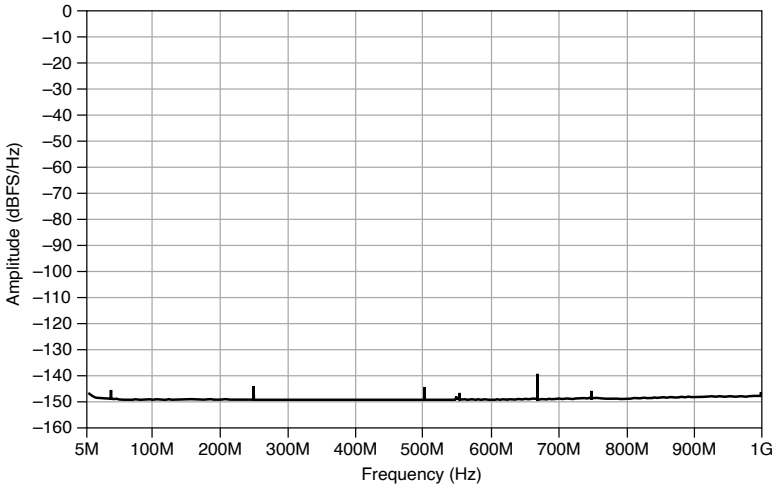
Figure 5. Measured Frequency Response[13], Unequalized, Digitizer Mode



Average Noise Density

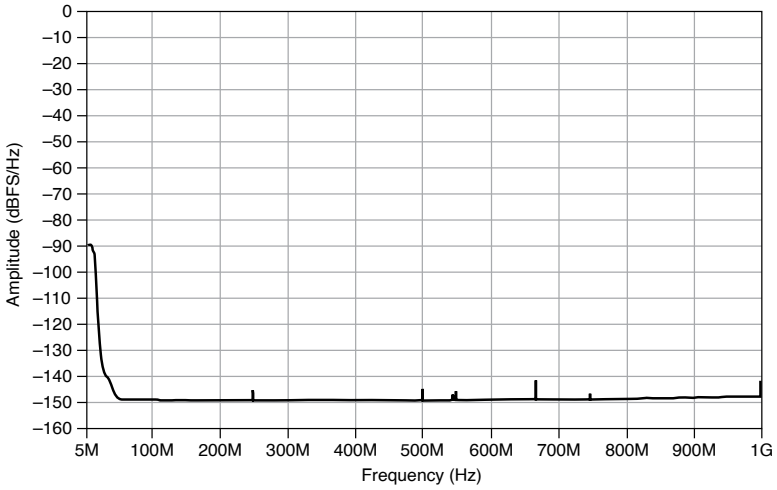
Average noise density	-149.5 dBFS/Hz, typical[14]

Figure 6. Measured Input Terminated Noise Density[15], Dither Off, Digitizer Mode



13. Conditions: Dither disabled, plot normalized to 10 MHz.
14. Conditions: Measured using digitizer mode, dither disabled, input terminated with a 50 Ω load, noise averaged and normalized to 1 Hz noise bandwidth.
15. Conditions: Averages = 500, RMS averaging, Flat Top window, 1 × 10 samples per average.

Figure 7. Measured Input Terminated Noise Density[16], Dither On, Digitizer Mode



Spurious Responses

Digitizer Mode

Effective number of bits (ENOB), typical[17][17]	
100 MHz	9.1
410 MHz	9.0
730 MHz	8.8
Signal-to-noise ratio (SNR), typical[17]	
100 MHz	57.5 dB
410 MHz	57 dB

16. Conditions: Averages = 500, RMS averaging, Flat Top window, 1 × 10 samples per average.
17. Conditions: Dither off, 8.1 dBm single tone at 100 MHz, 8.3 dBm single tone at 410 MHz, 8.7 dBm single tone at 730 MHz, 1,500 Hz resolution bandwidth (RBW).

730 MHz	56 dB
Spurious-free dynamic range (SFDR), typical[18]	
50 MHz to 1.5 GHz	-72 dBc
1.5 GHz to 2 GHz	-70 dBc
48 MHz	-77 dBc
100 MHz	-79 dBc
185 MHz	-80 dBc
410 MHz	-75 dBc
650 MHz	-75 dBc
730 MHz	-74 dBc
925 MHz	-74 dBc
Total harmonic distortion (THD), typical[19]	
50 MHz to 1.4 GHz	-72 dBc

18. Conditions: Dither on, 5 dBm single tone. SFDR is dominated by second and third harmonics.
19. Conditions: Dither on, 5 dBm single tone, second through sixth harmonics.

1.4 GHz to 2 GHz	-70 dBc
48 MHz	-76 dBc
100 MHz	-77 dBc
185 MHz	-78 dBc
410 MHz	-74 dBc
650 MHz	-75 dBc
730 MHz	-74 dBc
925 MHz	-74 dBc

DDC Mode

Third-order intermodulation distortion (IMD3), typical[20]	
50 MHz to 1 GHz	-75 dBc
1 GHz to 1.975 GHz	-68 dBc

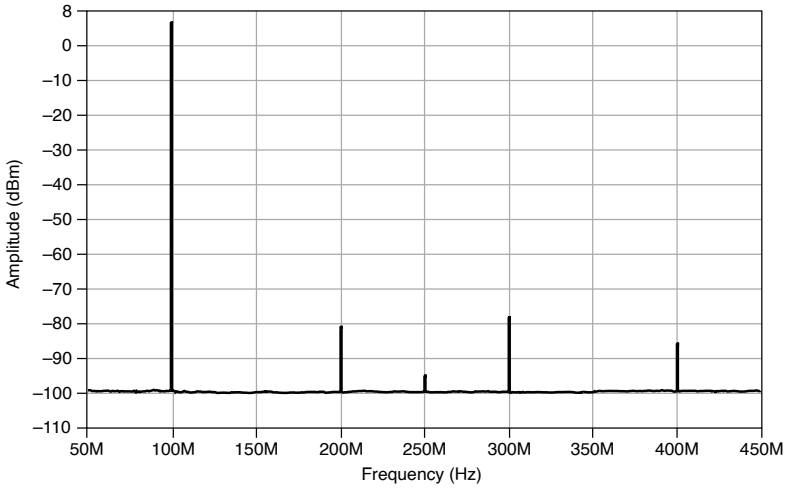
20. Conditions: Dither on, two -2 dBm tones spaced 1 MHz apart, I/Q rate = 8.75 MHz.

Table 6. Spurious-Free Dynamic Range (SFDR), Typical

Bandwidth (MHz)	Center Frequency (MHz)	SFDR (dBc)
100	187.5	-95[21]
400	730	-76[22]
30	500	-100, nominal
80	500	-100, nominal
100	500	-100, nominal
400	500	-87, nominal
800	500	-87, nominal

DDC out-of-band suppression	>85 dB [23]
DDC frequency shift SFDR	-105 dBFS

Figure 8. Measured Single-Tone Spectrum, 400 MHz Instantaneous Bandwidth, DDC Mode[24]



21. Conditions: Dither on, I/Q rate = 125 MHz.
22. Conditions: Dither on, I/Q rate = 500 MHz.
23. Stopband suppression from (0.6 × I/Q rate).
24. Conditions: Dither on, 500 MHz I/Q rate, 250 MHz frequency shift, 10 kHz noise bandwidth. 400 MHz acquisition FPGA image, 5 dBm single-tone input at 100 MHz.

Figure 9. Measured Single-Tone Spectrum, 800 MHz Instantaneous Bandwidth, DDC Mode[25]

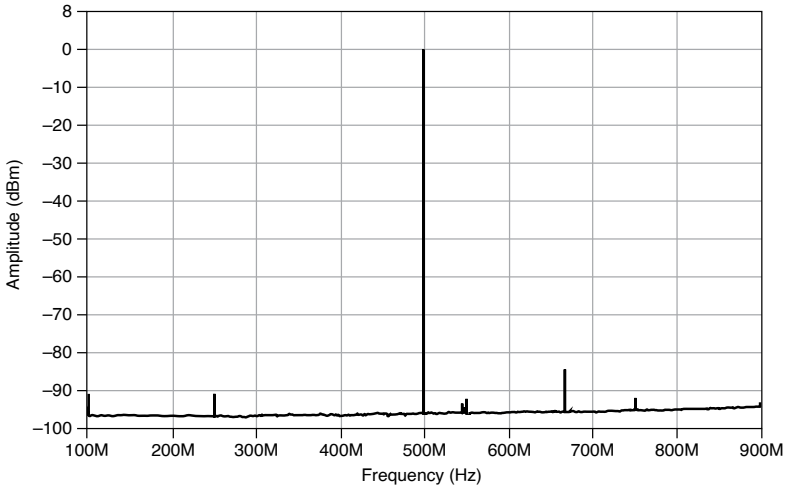
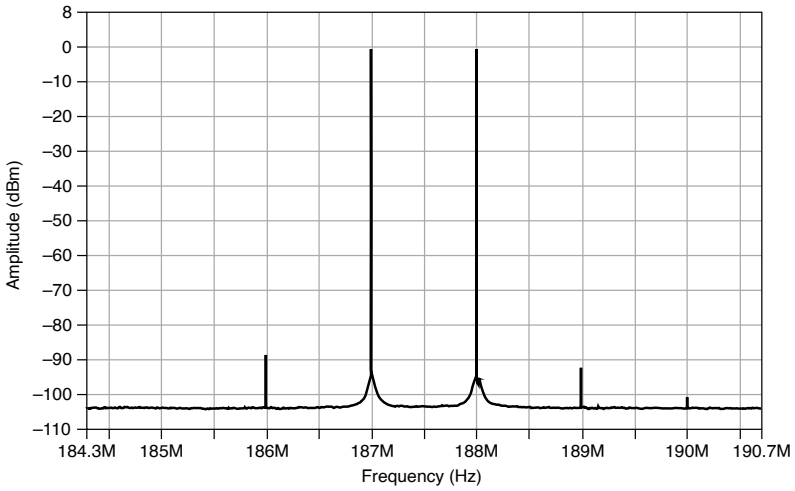
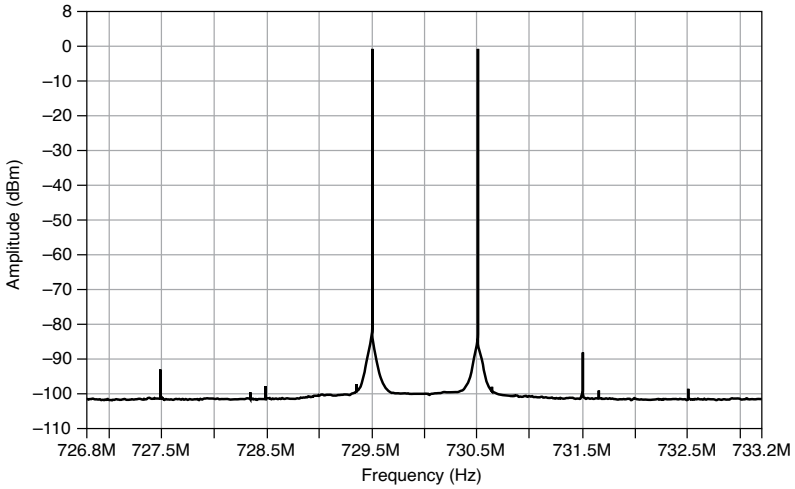


Figure 10. Measured Two-Tone Spectrum, 187.5 MHz Center Frequency, DDC Mode[26]



25. Conditions: Dither on, 1 GHz I/Q rate, 500 MHz frequency shift, 20 kHz noise bandwidth, 800 MHz acquisition mode FPGA image, 0 dBm single-tone input at 500 MHz.
26. Conditions: Dither on, 8 MHz I/Q rate, 187.5 MHz frequency shift, 4 kHz noise bandwidth, 400 MHz acquisition FPGA image, input is two -2 dBm tones spaced 1 MHz apart.

Figure 11. Measured Two-Tone Spectrum, 730 MHz Center Frequency, DDC Mode[27]



Error Vector Magnitude (EVM)

20 MHz bandwidth 64-QAM EVM[28]	
900 MHz	-51.5 dB, nominal
1.8 GHz	-50 dB, nominal

Digitizer Characteristics

Resolution	12 bits
Digitizer mode sample rate	2 GS/s
PXI Express Bus	PXI Express x8 Gen 2

27. Conditions: Dither on, 8 MHz I/Q rate, 730 MHz frequency shift, 4 kHz noise bandwidth, 400 MHz acquisition FPGA image, input is two -2 dBm tones spaced 1 MHz apart.
28. Conditions: EVM signal: 20 MHz bandwidth, 64-QAM signal, root-raised cosine pulse shape filtering, 0.25 alpha, internal Reference Clock source, 300 µs record length, PXIe-5644 used as signal generator, 2 dBm (average) power.

Onboard FPGA

FPGA	Xilinx Kintex-7 XC7K410T
Lookup tables (LUT)	254,200
Flip-flops	508,400
DSP48 slices	1,540
Embedded block RAM	28,620 kbits
Data transfers	DMA, interrupts, programmed I/O
Number of DMA channels	32

Onboard DRAM

Memory size	2 GB
Theoretical maximum data rate	6.4 GB/s

Onboard SRAM

Memory size	2 MB

Maximum data rate (read)	26 MB/s
Maximum data rate (write)	20 MB/s

Front Panel I/O

IF IN

Connector	SMA female
Input impedance	50 Ω, nominal
Coupling	AC
Absolute maximum input power	20 dBm, continuous wave (CW) RMS
Input return loss/VSWR	>15 dB/1.43:1 [29], typical

CLK IN

Connector	SMA female
Frequency	
Sample Clock	4 GHz, 2 GHz

29. 5 MHz to 2 GHz.

Reference Clock	100 MHz, 10 MHz
Tolerance	±50 ppm
Amplitude	
10 MHz and 100 MHz Reference Clocks	-3 dBm to 15 dBm[30]
2 GHz and 4 GHz Sample Clocks	-5 dBm to 10 dBm
Input impedance	50 Ω, nominal
Coupling	AC

CLK OUT

Connector	SMA female
Frequency	
Sample Clock	2 GHz
Reference Clock	100 MHz, 10 MHz[31]
Tolerance	Same as Reference Clock or Sample Clock source[32]

30. Optimal performance for a 10 MHz Reference Clock is greater than 4 dBm.
31. 100 MHz available when locking to CLK IN or PXIe_CLK100. 10 MHz available when locking to external front panel CLK IN.

Amplitude, typical	
Reference Clock (CLK IN)	CLK IN input power + 3 dB, nominal
Reference Clock (PXIe_CLK100)	7.5 dBm
Sample Clock	5 dBm
Output impedance	50 Ω, nominal
Coupling	AC

PFI 0 (Programmable Function Interface)

Connector	SMA female
Voltage levels	
Absolute maximum input range	-0.5 V to 5.5 V
V_{IL}	0.8 V
V_{IH}	2.0 V
V_{OL}	0.2 V with 100 µA load

32. Refer to the Internal Frequency Reference section for more information about internal frequency reference accuracy specifications.

V_{OH}	2.9 V with 100 µA load
Recommended operating voltage	0 V to 3.3 V
Input impedance	10 kΩ, nominal
Output impedance	50 Ω, nominal
Maximum DC drive strength	24 mA
Minimum required direction change latency	60 ns + 1 clock cycle[33]

AUX I/O

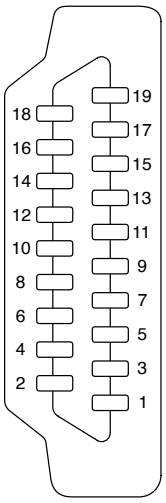
Connector	HDMI
Number of channels	12 digital input/output, bi-directional
Voltage levels	
Absolute maximum input range	-0.5 V to 5.5 V
V_{IL}	0.8 V
V_{IH}	2.0 V

33. ***Clock cycle*** refers to the FPGA clock domain used for direction control.

V_{OL}	0.2 V with 100 µA load
V_{OH}	2.9 V with 100 µA load
Input impedance	10 kΩ, nominal
Output impedance	50 Ω, nominal
Maximum DC drive strength	24 mA
Minimum required direction change latency	60 ns + 1 clock cycle[]
Maximum toggle rate	10 MHz
Recommended operating voltage	0 V to 3.3 V
5 V maximum current	10 mA
5 V voltage tolerance	4.2 V to 5.0 V

Table 7. PXIe-5624 AUX I/O Connector Pin Assignments

AUX I/O Connector	Pin	Signal	Signal Description
	1	DIO (0)	Bidirectional single-ended (SE) digital I/O (DIO) data channel.
	2	GND	Ground reference for signals.

AUX I/O Connector	Pin	Signal	Signal Description
	3	DIO (1)	Bidirectional SE DIO data channel.
	4	DIO (2)	Bidirectional SE DIO data channel.
	5	GND	Ground reference for signals.
	6	DIO (3)	Bidirectional SE DIO data channel.
	7	DIO (4)	Bidirectional SE DIO data channel.
	8	GND	Ground reference for signals.
	9	DIO (5)	Bidirectional SE DIO data channel.
	10	DIO (6)	Bidirectional SE DIO data channel.
	11	GND	Ground reference for signals.
	12	DIO (7)	Bidirectional SE DIO data channel.
	13	DIO (8)	Bidirectional SE DIO data channel.
	14	NC	No connect.
	15	DIO (9)	Bidirectional SE DIO data channel.
	16	DIO (10)	Bidirectional SE DIO data channel.
	17	GND	Ground reference for signals.
	18	+5 V	+5 V power (10 mA maximum).
	19	DIO (11)	Bidirectional SE DIO data channel.

Power Requirements

Table 8. Power Requirements[34]

Voltage (V_{DC})	Typical Current (A)	Maximum Current (A)
+3.3	2.45	2.75
+12	1.95	2.2 [34]

Calibration

Calibration interval	1 year

Note For a two-year calibration interval, add 0.1 dB to the one-year specifications for Absolute Amplitude Accuracy.

Physical Characteristics

Hot Surface If the PXIe-5624 has been in use, it may exceed safe handling temperatures and cause burns. Allow the PXIe-5624 to cool before removing it from the chassis.

PXIe-5624 module	3U, one slot, PXI Express module
Dimensions	21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)
Weight	454 g (16.0 oz)

34. Power consumption is 31.5 W, typical. Power consumed depends on FPGA image being used. Power specifications reflect the 400 MHz acquisition FPGA image. Maximum power consumption is at highest operating temperature.

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}

Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/`

environment/rohs_china.)